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LEAKAGE REDUCTION IN ONE BIT FULL ADDER USING SUB THRESHOLD LOGIC WITH BODY BIAS EFFECT

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Abstract— In recent years, sub-threshold logic and body bias technique provides ultra low power and high speed operation. Therefore, sub-threshold circuit design is very promising for future ultra low-energy sensor applications, pace maker as well as high-performance parallel processing. Sub-threshold logic is the new technique to overcome the problem of performance and delay. New methodology and topology is used for the designing of sub-threshold circuit. The main focus of this paper is to reduce the overall leakage by sub-threshold logic with body bias technique. We will design and simulate the 1 Bit full adder and see the result. Circuit simulations were conducted using 180nm CMOS technology to validate proposed concept. The results were compared with standard body bias technique in terms of leakage reduction.

Keywords: Sub-threshold logic; Body bias; low power;1 bit full adder

I. INTRODUCTION

Ultra low energy is required in today's electronic market for new trends of ultra low power circuit. Ultra-low power applications such as micro-sensor networks, pacemakers, and many Portable devices require extreme energy constraint for long battery life time. Sub-threshold operation presents an opportunity for such energy-constrained applications with its very low energy consumption.

Sub-threshold circuits offer a promising solution for implementing highly energy-constrained systems in clock ranges of low to medium frequencies for remote or mobile applications [1]. As the power supply voltage (Vdd) is scaled below the device threshold voltage (Vth), the sub-threshold current ever so slowly charges and discharges nodes for the circuit's logic function.

This weak driving current inherently limits the performance but minimum energy operation of the circuit is achieved with reduced dynamic and leakage power, resulting in long battery life in the past decades, sub-threshold circuit design was not well recognized in the area of digital circuits as high performance demand was a major concern. The low power design can increase operation time and/or utilize a smaller size and lighter-weight battery. One of the main reasons causing the leakage power increase is increase of sub threshold leakage power. When technology feature size scales down, supply voltage and threshold voltage also scale down. Sub threshold leakage power increases exponentially as threshold voltage decreases. The Body bias technique is used to improve the speed of the device. In the sub-threshold region therefore due to the absence of conducting inversion channels, transistors behave differently as compared to when they are operated in a normal strong inversion region.

This minute leakage current however limits the maximum performance at which the sub-threshold circuit can be operated. Sub-threshold operation sacrifices speed for power creating a clear divide between designing for high speed and ultra-low power. A majority of the work on sub-threshold has focused only on the ultra-low power aspect of this region treating speed as a secondary metric Body biasing techniques i.e. controlling the potential of bulk terminal of MOS transistor, can be used to bridge the speed and power gap in sub-threshold circuits.

A number of body biasing techniques have been proposed in literature for the sub-threshold logic Sub-threshold circuits are sensitive to manufacturing variability Body biasing also increases robustness in sub-threshold circuits. Low energy per operation is a primary design parameter in such applications.

II. MOTIVATION

Sub-threshold circuit design is suitably applicable for emerging portable applications that need tremendously low energy operation. Ultra low power is required in every device in today's electronic market [2]. The limitation of this technique is very slow speed of operation due to the extremely

scaled down supply voltage. Depending upon the application, size, weight and cost can be equally important as performance, especially for remote, portable and mobile applications, low-power has significance [3]. Reduced power consumption makes the circuits lighter, reduces or eliminates cooling subsystems, and reduces the weight and extends the life of the energy source .In this paper we have to reduce leakage current of the device. To provide a motivational scenario to illustrate the possible impact of this paper, let us compare the impact of static (leakage) power consumption. We can reduce the delay and power dissipation.

Although there already exist many low-leakage techniques, the best prior low-leakage technique in terms of leakage power reduction. Therefore, an ultra- low-leakage technique that can save state even in non-active mode can be quite important in nano-scale technology VLSI. To reduce overall leakage we introduce new technique sub-threshold logic with body bias effect.

III. OBJECTIVE AND SCOPE

Sub-threshold circuits operate with a supply voltage that is less than the threshold of the transistor—far below traditional levels and consequently the transistor operates essentially on leakage. While traditional digital CMOS has relied on running transistors either in the ON state (saturation) or OFF state (sub-threshold), sub-threshold circuits are either in an OFF state or an almost-ON state (still in sub-threshold regime but with weak inversion).

Running at these nonstandard operating points limits performance, which remains acceptable for low-to-medium cost applications given the substantial increase in the corresponding energy efficiency [4]. As power is related quadratic ally to the supply voltage, reducing the voltage to these ultra-low levels results in a dramatic reduction in both power and energy consumption in digital systems. Due to the exponential current-voltage (I-V) characteristics of the transistor, sub-threshold logic gates provide near ideal voltage transfer characteristics. The potential for minimizing energy at the cost of speed degradation defines the following set of applications for which sub-threshold circ circuits are well suited.

(a) Energy-constrained applications such as wireless sensor nodes, RFID tags, medical equipments such as hearing aids and pace-maker, wearable computing or implants, Personal digital assistants, energy scavenging applications, and Laptops, which are dominated primarily by the need to minimize energy consumption and increase battery life time, speed is a secondary consideration for this class of applications, so sub-threshold circuits offer a good solution.

(b) Many burst mode applications, requiring high performance for very short duration between extended periods of low-performance operation, Sub-threshold circuits can minimize energy for computations executed during the low-performance slots. This type of applications appears almost in every design, including the high-performance microprocessors, and cell phones.

3.1 Full adder

The one bit full adder circuit is one of the most widely used building blocks in all data processing (arithmetic) and digital signal processing architecture. The full adder operation can be stated as follows: Given the three 1-bit inputs A, B, and C, it is desired to calculate the two 1-bit outputs Sum and Carry,

Where,

Sum = (A **xor** B) **xor** C _____(1)

Cout = AB+BC+AC_____(2)

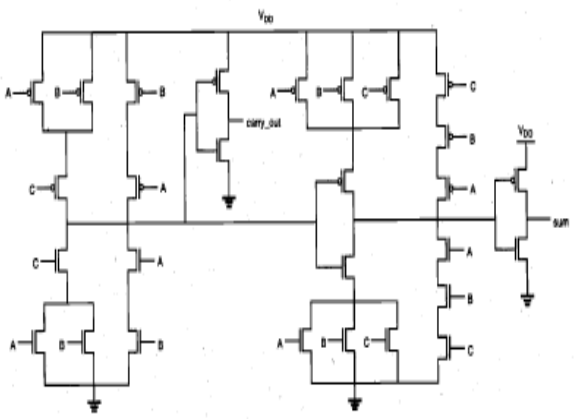

Fig 1: schematic of transistor level of 1 bit full adder

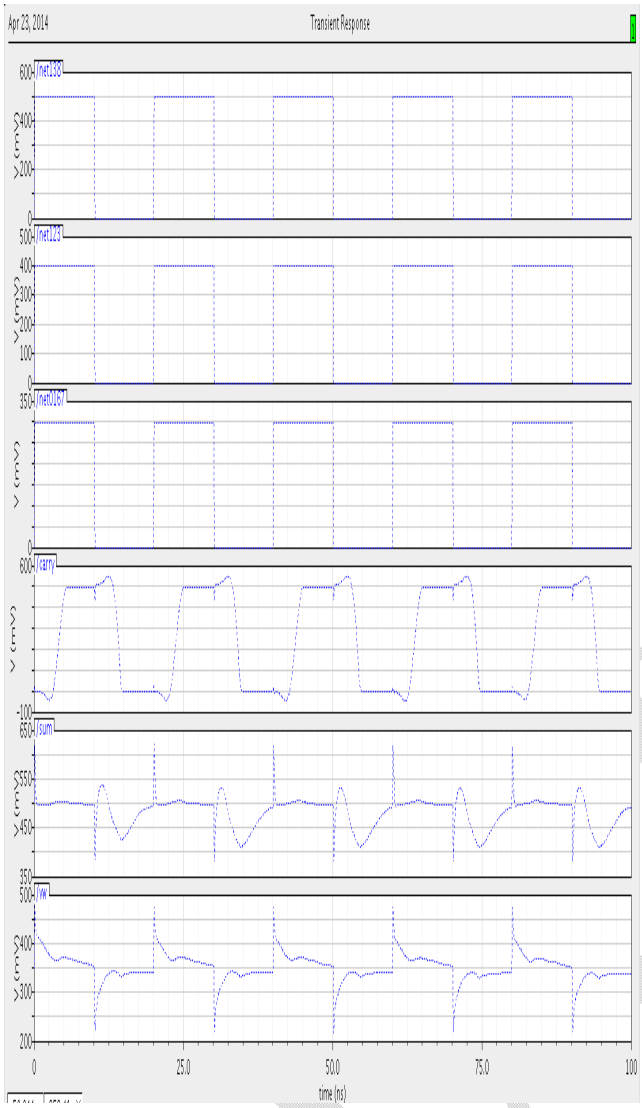

Fig 2: output response of one bit full adder with body bias

We use Count signal to generate the sum output. This implementation will ultimately reduce the circuit complexity and hence, save chip area. The circuit contains 14 NMOS and 14 PMOS transistor, together with the cmos inverter to generate output. The leakage is reduces by apply the sub-threshold logic and speed can be in increase by body bias effect. We use 3 inputs A, B, C and an inverter at output to generate output. There are 14 nmos and 14 pmos transistor in 1 bit full adder.

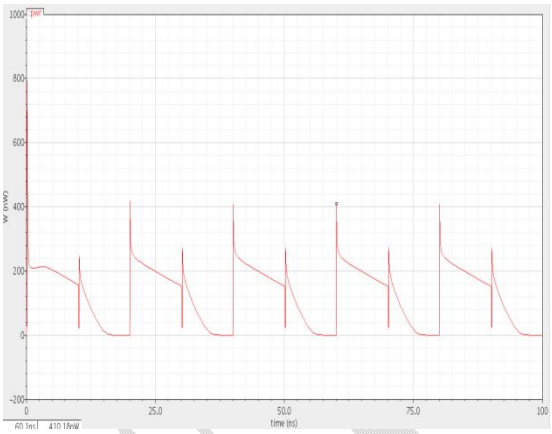

Fig 3: power in one bit full adder with body bias

IV. CONCLUSION

The 1 bit full adder with sub-threshold logic is used to reduce the leakage in NMOS and PMOS transistors in inverter. Simulation results were obtained using 180nm technology assuming near minimum and same sized NMOS and PMOS transistors. Circuit is simulated for VDD= 0.5V and Vin=0.3V. Due to the body effect, the lowering of VW reduces the threshold voltage of NMOS and increases threshold voltage of PMOS. This in turn results in faster pull-down operation similarly due to the body effect; the increasing of VW increases the threshold voltage of NMOS and decreases the threshold voltage of PMOS. This in turn results in faster pull up operation. The power consumption is calculated by applying body bias is124.5E-9 which is less than of power without body bias 126.4E-9.

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